# Electrical Characterization of Defects in $Al_2O_3$

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The dielectric properties of atomic layer deposited pure $Al_2O_3$ and Si doped $Al_2O_3$ thin films were characterized by various measurement techniques. By the use of capacitance voltage and conductance measurements charged defects within the oxide and at the silicon interface were detected. It was shown that the passivation quality of $Al_2O_3$ is strongly related to the density of fixed oxide charges $Q_f$ and the interface trap density $D_{it}$. The fixed charge density could be adjusted from $-6.2 \cdot 10^{12}$ $cm^{-2}$ for samples annealed at 500°C to $+2.1 \cdot 10^{12}$ $cm^{-2}$ for as deposited Si doped layers.
Additionally current voltage characteristics were performed in a temperature range from 25°C to 125°C. The leakage current was found to increase with higher temperature. A barrier height of 0.4 eV was extracted from the data by assuming a Pool-Frenkel mechanism.

## Introduction

High-k dielectrics play a major role in semiconductor research and development. The semiconductor industry faces nanocrystalline dielectrics for metal-insulator-metal (MIM) capacitors in DRAM devices (1) and rf applications, as well as for gate dielectrics in sub 45 nm devices. Also high-efficiency solar cells rely on the excellent passivation properties of high-k thin films like $Al_2O_3$ (2, 3). However, the use of high-k dielectrics instead of $SiO_2$ leads to new effects like charge trapping, stress induced leakage currents (4, 5), change in the field extrapolation model of lifetime (6) and an increase of dielectric absorption effects (7). Most of the described effects are connected to the formation of defect states within the bandgap of the dielectric material. Depending on the application these effects can be undesirable or highly beneficial as we will show it for $Al_2O_3$ passivation layers on solar cells.

In this work we will review our electrical characterization studies on the example of $Al_2O_3$ as one important high-k representative. Therefore capacitance voltage measurements and conductance measurements will be shown for atomic layer deposited (ALD) thin films of $Al_2O_3$. From these methods the densities of fixed oxide charges $Q_f$ and interface states $D_{it}$ were extracted and their influence on the effective charge carrier lifetime $\tau_{eff}$ for solar cell application was pointed out. It was shown that the amount of fixed charges and interface traps can be controlled by the deposition conditions and a subsequent anneal.

Additionally a sample set with silicon doped $Al_2O_3$ was produced in order to stabilize the amorphous phase and increase the recrystallization temperature of the dielectric as it was shown for $HfO_2$ (8). It was found that by the incorporation of Si into the dielectric the fixed charge density could be adjusted further which can be used for specific defect-engineering.

## Experimental

Sample Preparation

Two different sample sets (Table I) were prepared by ALD on float-zone *n*-type Si substrates with a resistivity of 2-3 Ω·cm. Before deposition of the $Al_2O_3$ the samples were treated by a standard cleaning procedure. The first cleaning step (SC1) with a solution of $NH_4OH$, $H_2O_2$ and deionized water at the ratio of 1:1:5 for 10 minutes at 80°C was performed to remove organics and particles. Whereas the second cleaning step (SC2, $HCl:H_2O_2:H_2O$ at the ratio of 1:1:5, 10 min at 80°C) should remove remaining metallic contaminants. After the cleaning procedure all samples were exposed to diluted HF for 60 s in order to strip the native oxide. After sample drying the $Al_2O_3$ or Si doped $Al_2O_3$ layers were deposited symmetrically on both sides.

Sample set A was produced at Hanwha Q Cells by an ALD process based on the precursors trimethylaluminium (TMA) and ozone ($O_3$). After deposition the samples of subset A1 were annealed at temperatures from 300 to 600°C for 10 min in a muffle furnace. It was found that the best passivation behavior occurred at an annealing temperature of 470°C. Subset A2 was therefore annealed at 470°C for 10 min in various pure atmospheres ($N_2$, $H_2$ and $O_2$) in a cleanroom grade diffusion furnace. A detailed description of the deposition process can be found elsewhere (3).

Sample set B was fabricated using an Ultratech Savannah S200 system and a TMA and $H_2O$ based ALD process. Additionally, the samples were Si doped by replacing a fraction of the TMA pulses by silanediamine (SAM) pulses. The ratio of SAM to TMA pulses ranged from 0:11 for pure $Al_2O_3$ to 1:1. Set B was not annealed after deposition.

**TABLE I.** Sample overview for set A and B. Temperature and atmosphere refer to a 10 min post deposition anneal.

| Sample set | Si doping [SAM:TMA] | Thickness [nm] | Temperature [°C] | Atmosphere |
|---|---|---|---|---|
| A1 | - | 30 | 300-600 | air |
| A2 | - | 30 | 470 | $N_2$, $H_2$, $O_2$ |
| B | 0:11 to 1:1 | 24-37 | as dep. | - |

Contact formation for electrical characterization was carried out after dielectric deposition and sample annealing. Therefore a top electrode consisting of 5 nm Ti and 100 nm Al was deposited by electron beam evaporation through a shadow mask. The minority carrier lifetime $\tau_{eff}$ was determined by transient decay photoconductance technique (QSSPC) on a Sinton Instruments WCT-120 system prior to the metal deposition. Capacitance voltage (CV), conductance and temperature dependent current voltage (IV) measurements were performed on the resulting metal insulator semiconductor (MIS) structures.

Extraction of $Q_f$ from CV Measurements

High frequency CV measurements of sample set A and B were performed at 100 kHz. With a nonlinear least-squares regression routine the data was fitted to an ideal CV characteristic and the relevant parameters were extracted following (9, 10). The substrate doping concentration $N_D$ was calculated by the depletion layer capacitance $C_D$ [1]. Where q is the elemental charge, $\varepsilon_{si}$ is the permeability of the silicon and V is the applied voltage.

$$N_D = -\frac{2}{q \cdot \varepsilon_{si}} \left( \frac{d 1/C_D^{\,2}}{dV} \right)^{-1} \qquad [1]$$

The fixed charge density is determined by the offset of the flatband voltage $V_{FB}$ [2]. Where $\phi_{ms}$ is the work function difference between the top electrode and the silicon substrate and $C_{is}$ is the insulator capacitance extracted from the accumulation region.

$$Q_f = (\phi_{ms} - V_{FB}) \cdot C_{is} \qquad [2]$$

The work function difference $\phi_{ms}$ for an *n*-type Si is given by [3] where $\phi_m$ is the metal work function, $\chi$ the silicon electron affinity, $E_g$ the width of the silicon energy gap, k the Boltzmann constant, T the temperature and $n_i$ the intrinsic charge carrier density.

$$\phi_{ms} = \phi_m - \left( \chi + E_g/2q - kT/q \cdot \ln(N_D/n_i) \right) \qquad [3]$$

The flatband condition occurs when the measured capacitance reaches the semiconductors flatband capacitance $C_{FB}$ [4]. Where $\varepsilon_{is}$ and $d_{is}$ are the insulator permeability and thickness and $L_D$ is the Debye length of the semiconductor. In flatband condition the applied bias voltage is equal to $V_{FB}$.

$$C_{FB} = \frac{\varepsilon_{is} \cdot \varepsilon_{si}}{\varepsilon_{si} \cdot d_{is} + \varepsilon_{is} \cdot L_D} \qquad [4]$$

## Results and Discussion

Impact of $Q_f$ on Surface Passivation

Figure 1a shows the effective minority carrier lifetime $\tau_{eff}$ of sample set A in dependency of the excess carrier density $\Delta n$ (3). The data was acquired by the QSSPC technique. The sample annealed at 300°C showed a low effective lifetime. A higher lifetime could be achieved only after annealing at temperatures above 400°C. The best result at an injection of $10^{14}$ $cm^{-3}$ was achieved after an anneal at 470°C. Apparently the samples from subset A2 annealed in pure atmosphere showed a higher $\tau_{eff}$ than the samples annealed in the muffle furnace. This is due to defects in the silicon bulk material which are likely to be generated by diffusion of contaminants within the muffle furnace.

In Figure 1b the dependency between the extracted $Q_f$ and $\tau_{eff}$ is shown. The fixed oxide charge at the $Al_2O_3$/Si interface is negative and its absolute value increases for higher annealing temperatures up to 500°C. An increase in $Q_f$ leads to better surface passivation due to the majority charge carrier depletion caused by the repelling electric field effect. This results in an overall increase of $\tau_{eff}$. Only for subset A1 where $\tau_{eff}$ is dominated by silicon bulk defects a further increase in $Q_f$ does not result in a higher minority carrier lifetime. The highest lifetime of 9.0 ms at an injection level of $10^{14}$ $cm^{-3}$ was achieved for the sample annealed for 10 min at 470°C in $O_2$. This value is close to the intrinsic lifetime limit of 10.5 ms for *n*-type Si according to (11). Although the samples annealed in $N_2$ and $H_2$ exhibit a similar $Q_f$ the corresponding $\tau_{eff}$ is significantly lower. A possible explanation would be a difference in the chemical passivation of the $Al_2O_3$/Si interface. Therefore conductance measurements which are very sensitive to interface properties (10) were carried out.

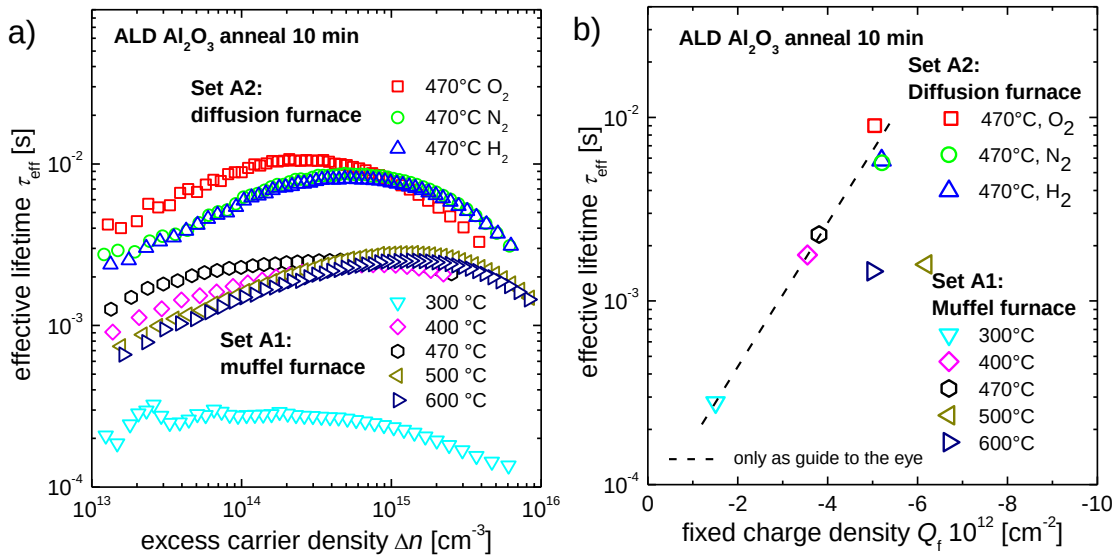


Figure 1. a) Effective lifetime $\tau_{eff}$ as function of the injection level after annealing for 10 min at different temperatures in varying atmospheres, b) $\tau_{eff}$ as function of the fixed charge density at an injection level of $10^{14}$ $cm^{-3}$ (adapted from (3)).

## Impact of Interface Traps on Surface Passivation

Conductance Measurements were performed in order to extract the interface trap density. Therefore the conductance $G_m$ was measured in parallel to the capacitance $C_m$ at frequencies from 1 kHz to 1 MHz (Figure 2a). The voltage was swept in the depletion region which is known from the CV data acquired previously. To correct the measurement data for the insulator capacitance $C_{is}$ and any parasitic series resistance $R_S$ a conductance measurement in accumulation was performed first. The equivalent circuit for the samples is shown in Figure 2b.

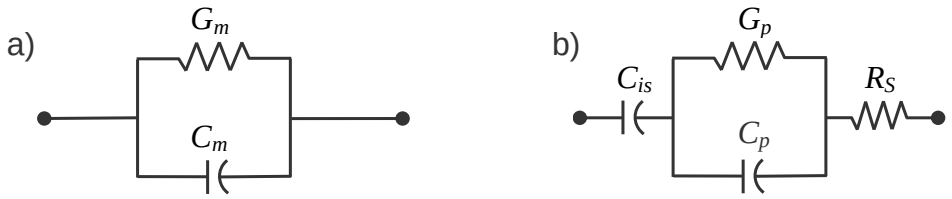


Figure 2. a) Equivalent circuit for the measured values $C_m$ and $G_m$, b) equivalent circuit including the insulator capacitance and a parasitic series resistance (10).

The extracted conductance $G_p$ per angular frequency $\omega$ is plotted versus frequency (Figure 3). It can be seen that there is a shift of the peak position and a change in its amplitude when the bias voltage is swept from weak inversion towards flatband. The characteristics are described by [5] as proposed by (10). Where $\tau_{it}$ is the interface trap time constant and $P(U_S)$ is attributed to a peak broadening by fluctuations of the normalized surface potential $U_S$ [6].

$$\frac{Gp}{\omega} = \frac{q}{2}\int_{-\infty}^{+\infty}\frac{D_{it}}{\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]P(U_S)dU_S \qquad [5]$$

$$P(U_S) = \frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{(U_S-\overline{U}_S)^2}{2\sigma^2}\right) \qquad [6]$$

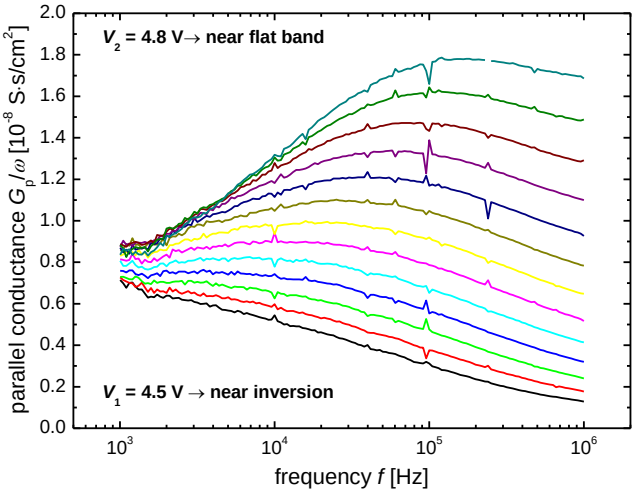


Figure 3. Extracted parallel conductance $G_p/\omega$ for different bias voltages in depletion for the $O_2$ annealed sample. The peak height and position shifts due to the bias voltage dependent response of the interface traps.

A nonlinear least square fitting routine was used to extract $D_{it}$ as a function of the applied bias voltage (Figure 4a). In order to determine the corresponding trap energies an additional low frequency CV measurement at 50 Hz was performed (Figure 4b). At low frequencies all interface traps will follow the applied ac signal and therefore $U_S$ and the interface trap energy $E_{it}$ can be calculated from the depletion region.

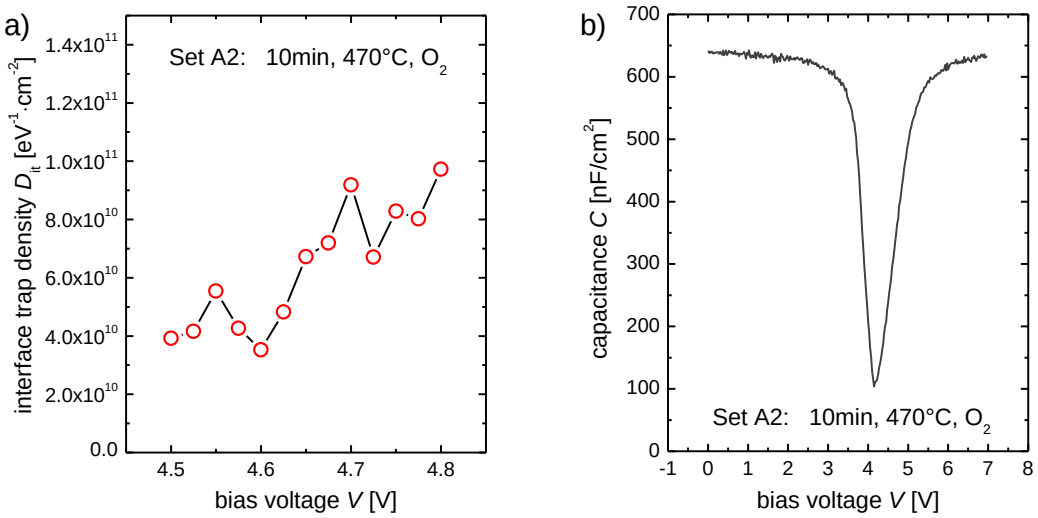


Figure 4. a) Extracted interface trap density $D_{it}$ as function of bias voltage V, b) low frequency CV characteristic measured at 50 Hz.

The resulting interface trap density for subset A2 and one sample from subset A1 annealed at 470°C in the muffle furnace are shown in Figure 5. It was found that the latter one showed the highest $D_{it}$. The samples annealed in $N_2$ and $H_2$ showed slightly lower interface trap densities, whereas the oxygen annealed sample exhibits the lowest $D_{it}$ of $5 \cdot 10^{10}$ $eV^{-1}cm^{-2}$ at 100 meV from midgap. These results (Table II) are in very good agreement with the lifetime measurements where the $O_2$ annealed sample performed best although the incorporated fixed charges density was similar to the $N_2$ and $H_2$ annealed samples. We believe that during the $O_2$ anneal the interface traps which are related to the interruption of the periodic lattice structure of the silicon substrate (12) are neutralized. However, ellipsometry measurements showed that the thickness of the dielectric layer did not increase after annealing, thus a simple oxidation of the substrate surface can be excluded.

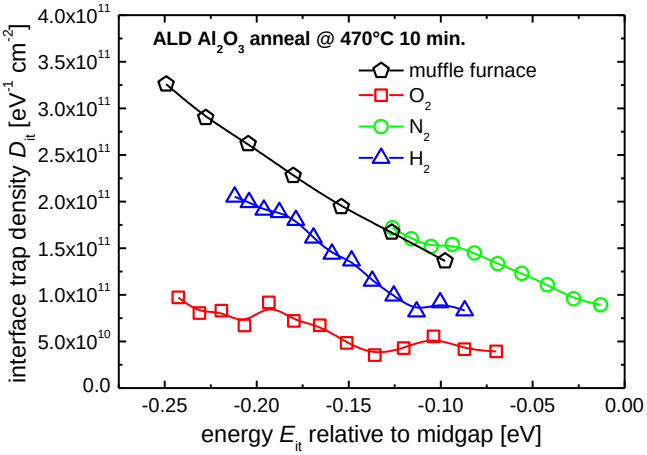


Figure 5. Comparison of the interface trap density for samples annealed at 470°C for 10 min. The $O_2$ annealed sample exhibits the lowest $D_{it}$ (adapted from (3)).

**TABLE II.** Results of the CV and conductance measurements. A high density of fixed charges and low $D_{it}$ leads to an excellent sample passivation measured in terms of $\tau_{eff}$.

| Temperature [°C] | Atmosphere | $Q_f$ [$10^{12}$ $cm^{-2}$] | $D_{it}$ @ 0.1 eV [$10^{11}$ $eV^{-1}cm^{-2}$] | $\tau_{eff}$ [ms] |
|---|---|---|---|---|
| 300 | air | -1.5 | - | 0.3 |
| 400 | air | -3.6 | - | 1.8 |
| 470 | air | -3.8 | 1.4 | 2.3 |
| 500 | air | -6.2 | - | 1.6 |
| 600 | air | -5.0 | - | 1.5 |
| 470 | $N_2$ | -5.2 | 1.5 | 5.8 |
| 470 | $H_2$ | -5.2 | 0.9 | 5.6 |
| 470 | $O_2$ | -5.1 | 0.5 | 9.0 |

Impact of Si Doping on the fixed Charge Density

Sample set B for the investigation on the effect of Si doping towards the fixed charge density was prepared using a TMA/$H_2O$ ALD process. In previous studies it was found that the fixed charge density using the $H_2O$ based process is at least one order of magnitude lower than for the TMA/$O_3$ process shown before. For as deposited samples $Q_f$ was $+2.0 \cdot 10^{11}$ $cm^{-2}$ compared to $-2.0 \cdot 10^{12}$ $cm^{-2}$ for the ozone based process. The slightly positive charge in case of the $H_2O$ based process can result from an incomplete removal of the native oxide. By the incorporation of Si into $Al_2O_3$ one would expect an additional contribution of positive fixed charges (9, 10).

Figure 6a shows the measured CV characteristics of the Si doped samples. The doping ratio of 0:11 denotes a pure $Al_2O_3$ layer, whereas a ratio of 1:10 implies that each eleventh TMA pulse was replaced by a SAM pulse. The chemical composition was analyzed by Rutherford backscattering (RBS, Table III). The CV characteristic of the undoped sample is only slightly shifted towards negative bias, whereas the Si doped samples exhibit a clear shift in flatband voltage. The accumulation capacitance for each measurement differs due to minor thickness variations between the samples.

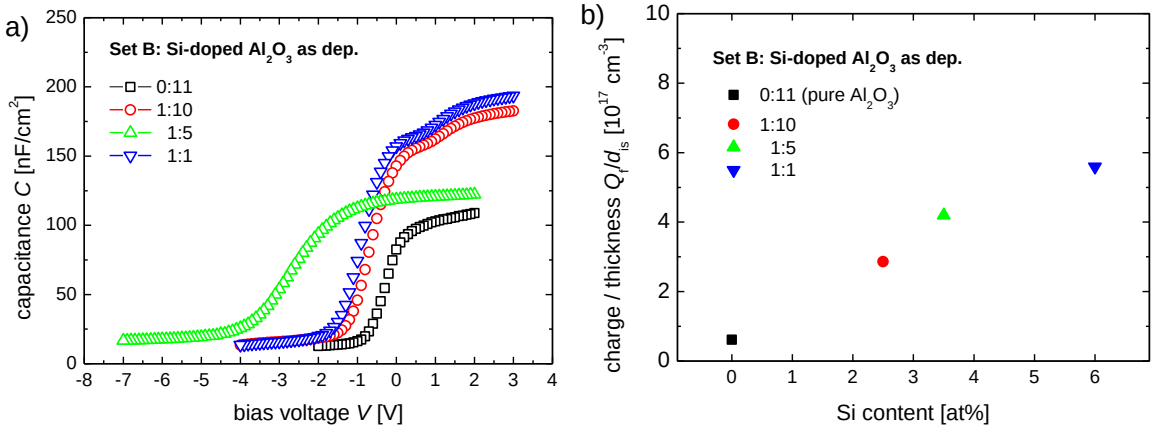


Figure 6. a) CV characteristic at 100 kHz for sample set B, Si doping leads to a negative shift of the flatband voltage, b) extracted fixed charge density per $Al_2O_3$ layer thickness.

**TABLE III.** Results of the RBS measurements for sample set B. The silicon content increases with higher doping ratio.

| Doping Ratio | Al Content [at%] | Si Content [at%] | O Content [at%] |
|---|---|---|---|
| 0:11 | 39,0 | 0,0 | 61,0 |
| 1:10 | 36,0 | 2,5 | 61,5 |
| 1:5 | 33,5 | 3,5 | 63,0 |
| 1:1 | 26,5 | 6,0 | 67,5 |

In Figure 6b the fixed oxide charge per sample thickness is shown. There is a clear trend towards increasing positive oxide charge for higher Si doping ratios. At higher doping ratios the number of Si rich layers per thickness is increased. It is assumed that the total oxide charge correlates with the Si content due to a positive charged defect introduced by the silicon (9, 10).

## Temperature dependent IV Measurements

Temperature dependent IV measurements were carried out for the $O_2$ annealed sample of subset A2 in order to determine the leakage current mechanism. Therefore the electrical field across the $Al_2O_3$ layer was calculated from the applied bias voltage and the surface potential of the silicon derived from the CV data. In a field region of 0 to 3 MV/cm the leakage current exhibits a strong temperature dependency (Figure 7a). The current density J increases with higher temperature. We found that in a field range of 0.25 to 1 MV/cm the current follows a Poole-Frenkel (PF) behavior [7] as it was reported by (13). Where E is the electric field, $\varphi_B$ is the barrier height and $C_1$ and $C_2$ are constants (9).

$$J = C_1 \cdot E \cdot \exp\left[\frac{q}{kT}\left(C_2\sqrt{E} - \varphi_B\right)\right] \qquad [7]$$

For the determination of the barrier height ln(J/E) was plotted versus $E^{1/2}$ (Figure 7b). The calculation resulted in a barrier of $\varphi_B$ = 0.40 eV. The leakage mechanism for higher electric field strengths needs further investigation. A possible explanation would be trap assisted tunneling (TAT).

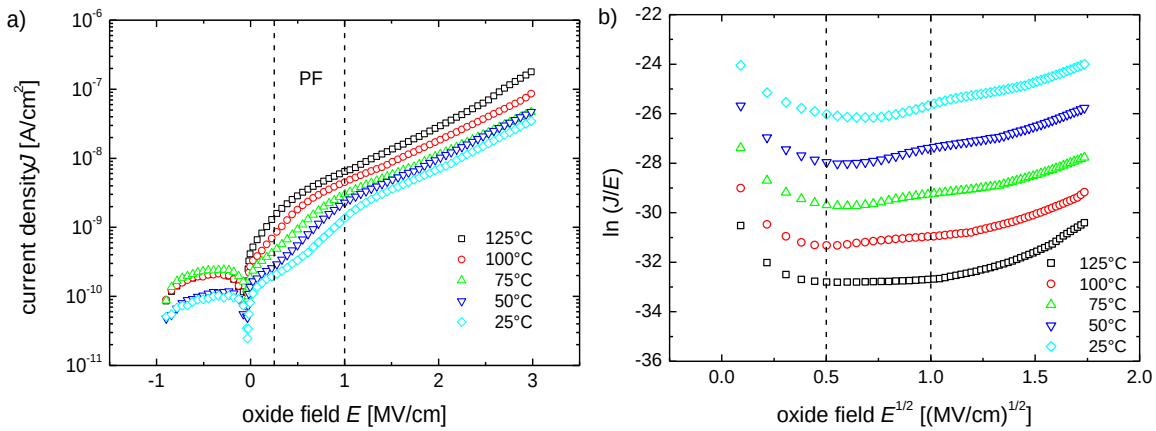


Figure 7. a) Temperature dependent IV characteristics of the $O_2$ annealed pure $Al_2O_3$ sample, b) Poole-Frenkel plot for the calculation of the barrier height $\varphi_B$.

## Conclusions

By the help of CV, conductance and IV measurement techniques the dielectric properties and defects of ALD deposited $Al_2O_3$ and Si doped $Al_2O_3$ thin films were studied. We showed that the fixed charge density of these layers can be varied in a wide range. Depending on the ALD process parameters, post deposition anneal and Si content the amount of $Q_f$ could be varied between $-6.2 \cdot 10^{12}$ $cm^{-2}$ and $+2.1 \cdot 10^{12}$ $cm^{-2}$, which is crucial for many applications. The effectivity of solar cell passivation layers on *n*-type Si increased drastically at high levels of $Q_f$. The best $\tau_{eff}$ of 9.0 ms at an injection level of $10^{14}$ $cm^{-3}$ was achieved for $Al_2O_3$ layers deposited with a TMA/$O_3$ ALD process and a subsequent anneal for 10 min in $O_2$. Furthermore a significant impact of the interface trap density on the passivation quality was detected. The lowest measured $D_{it}$ of $5 \cdot 10^{10}$ $eV^{-1} \cdot cm^{-2}$ is correlated to the highest $\tau_{eff}$ (3).

For microelectronic applications like the submicron field effect transistor a low $Q_f$ is desirable (9). By using a TMA/$H_2O$ ALD process low $Q_f < 2 \cdot 10^{11}$ $cm^{-2}$ could be achieved. However, even a positive $Q_f$ could be generated by doping of the $Al_2O_3$ with Si. The amount of positive charges increases with increasing Si content. Doped $Al_2O_3$ layers with positive $Q_f$ can be used for field effect passivation on *n*-type Si. Due to the electrostatic repulsion of minority charge carriers from the silicon surface an excellent surface passivation is expected (14).

Temperature dependent IV measurements were performed to determine the leakage current mechanism in $Al_2O_3$. The sample with the highest $\tau_{eff}$ and high negative $Q_f$ showed a strong increase of the leakage current with increasing temperature. At low electric fields between 0.25 and 1 MV/cm the current follows a Poole-Frenkel model. For this field region a barrier height of 0.40 eV was extracted. Further investigations on the correlation between $Q_f$, leakage current and defect energy levels in $Al_2O_3$ thin films will be done.

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